IN THE SPECIFICATION:

Please replace paragraph number **[0001]** with the following rewritten paragraph:

[0001] This application is a divisional of application Serial ~~No.~~ No. 10/118,366, filed April 8, 2002, pending.

Please replace paragraph number **[0003]** with the following rewritten paragraph:

[0003] In order to conserve the amount of surface area, or "real ~~estate",~~ estate," consumed on a carrier substrate, such as a circuit board, by semiconductor devices connected thereto, various types of increased density packages have been developed. Among these various types of packages is the so-called "multi-chip module" (MCM). Some types of multi-chip modules include assemblies of semiconductor devices that are stacked one on top of another. The amount of surface area on a carrier substrate that may be saved by stacking semiconductor devices is readily apparent-a stack of semiconductor devices consumes roughly the same amount of real estate on a carrier substrate as a single, horizontally oriented semiconductor device or semiconductor device package.

Please replace paragraph number **[0009]** with the following rewritten paragraph:

[0009] Different electrical connection technologies, including wire bonding, ~~tape-~~ tape-automated bonding ("TAB"), and controlled-collapse chip connection ("C-4"), which results in a so-called flip-chip arrangement, are but a few of the ways in which discrete conductive elements may be formed in stacked multi-chip modules. Different electrical connection technologies have also been used in single multi-chip modules, with the bond pads of one semiconductor device being electrically connected to corresponding contact areas of a carrier substrate of the multi-chip module with a different type of discrete conductive element than that used to form electrical connections between the bond pads of another semiconductor device and their corresponding contact areas of the carrier substrate.

Please replace paragraph number **[0044]** with the following rewritten paragraph:

[0044] Portions of base substrate 41 that underlie conductive traces 45 may electrically isolate conductive traces 45 from an active surface 32 of an underlying semiconductor device 30 (FIGs. 3 and 4). Alternatively, or in addition, at least portions of bottom side 43 of base substrate 41 may be coated with an adhesive material 48, such as a thermoset resin or a ~~pressure-~~ pressure-sensitive adhesive. Such a coating of adhesive material 48 may facilitate securing of rerouting element 40 to an active surface 32 of a semiconductor device 30 (FIGs. 3 and 4). Adhesive material 48 may also electrically insulate conductive traces 45 and contact pads 47 from underlying features of a semiconductor device 30 upon which rerouting element 40 is positioned, or provide an additional insulative layer or standoff distance that decreases or eliminates any electrical interference that may occur between semiconductor device 30 and conductive traces 45 or contact pads 47.